

PATENT APPLN. NO. 10/501,522  
RESPONSE UNDER 37 C.F.R. §1.111

**PATENT  
NON-FINAL**

**REMARKS**

The title has been amended. The amendment to the title is the same as that made to the title in a preliminary amendment filed in the present application on July 16, 2004. However, it appears that the amendment to the title made in the preliminary amendment has not been entered. Please amend the title at this time.

Claims 16-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsui et al., U.S. Patent No. 6,060,344 (hereinafter: "Matsui").

The Office's position is believed to be that the rejected claims read on, i.e., include within their scope, the semiconductor substrate and method disclosed in Matsui. This position appears to be related to a broad interpretation of the terms "cavities" and "cavity" in the rejected claims. The Office has identified the the concave portion 2 and the trenches 3 shown in Fig. 1G, which are filled with poly-crystal silicon, as "cavities" within the meaning of that term as recited in claims 16-21.

Applicants respectfully submit that the Office's interpretation is not proper.

First, although the Office is permitted to give claims their broadest reasonable interpretation, such interpretation must be consistent with the interpretation that a person of ordinary skill

PATENT APPLN. NO. 10/501,522  
RESPONSE UNDER 37 C.F.R. §1.111

**PATENT  
NON-FINAL**

in the art would give to the claims from a reading of the specification. In the present case, the terms "cavities" and "cavity" are used to mean open, or unfilled, spaces.

Second, the interpretation of the Office is inconsistent with the meaning given by Matsui to the concave portion 2 and the trenches 3 in Fig. 1G. Matsui describes the state in which the concave portion 2 and the trenches 3 in Fig. 1G are filled with poly-crystal silicon as being a "state in which there is no cavity" (Col. 7, lines 14-15).

Third, the cavity and trenches of Matsui filled with poly-crystal silicon do not comprise an insulating layer because the poly-crystal silicon conducts electricity.

Matsui also fails to disclose a step of "bonding said active layer wafer and said supporting substrate wafer to each other with said surface(s) having said recessed portion(s) formed therein serving as bonding surface(s) to thereby form a cavity" as recited in claim 18 of the application.

For the above reasons, Matsui is insufficient to support a case of anticipation under 35 U.S.C. § 102 of claims 16-21 and removal of the 35 U.S.C. § 102 rejection of these claims is in order.

PATENT APPLN. NO. 10/501,522  
RESPONSE UNDER 37 C.F.R. §1.111

**PATENT  
NON-FINAL**

Regarding the 35 U.S.C. § 103(a) rejection of claim 22 as being unpatentable over Matsui in view of Doyle, U.S. Patent No. 6,124,185, this rejection depends on the propriety of the rejection of claims 16-21 as being anticipated by Matsui. Since Matsui fails to support a case of anticipation of claims 16-21 under 35 U.S.C. § 102 for the reasons explained above, claim 22, which depends on claim 18, is prima facie patentable.

Removal of the 35 U.S.C. § 103(a) rejection of claim 22 is also in order.

Claims 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsu, U.S. Patent No. 6,114,197 (hereinafter: "Hsu").

The Office's position is apparently that the SOI substrate in Hsu is a bonded SOI substrate having a varied thickness.

Claim 23 has been amended to recite that a cavity is formed at the bonding interface between the SOI layer and the supporting substrate wafer.

Claims 23-26 as amended are directed to a semiconductor device comprising a bonded SOI substrate where a cavity is formed at the bonding interface between the SOI layer and the supporting substrate wafer. Hsu discloses a SIMOX substrate or a SOI wafer. There is no description in Hsu of a device including a bonded SOI substrate. Moreover, in the device of the present invention, a

PATENT APPLN. NO. 10/501,522  
RESPONSE UNDER 37 C.F.R. §1.111

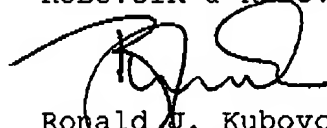
**PATENT  
NON-FINAL**

cavity is formed at the bonding interface between a SOI layer and a supporting substrate wafer. In Hsu a cavity is formed between blocks (Fig. 6; Col. 3, lines 50-60).

For these reasons, Hsu does not support a case of anticipation of claims 23-25 and removal of the 35 U.S.C. 102(b) rejections of claims 23-26 is also in order.

In the event that this paper is not considered to be timely filed, applicants hereby petition for an appropriate extension of time. The fee for any such extension and for any additional fees may be charged to our Deposit Account No. 111833.

Respectfully submitted,  
KUBOVCIK & KUBOVCIK



Ronald U. Kubovcik  
Reg. No. 25,401

Atty. Case No. ABE-025  
The Farragut Building  
Suite 710  
900 17th Street, N.W.  
Washington, D.C. 20006  
Tel: (202) 887-9023  
Fax: (202) 887-9093  
RJK/jbf